AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for forming a passivation layer on a memory device with an interconnect structure thereon, comprising:

providing a plurality of metal interconnect structures;

~~forming a substantially planarized inter-layered dielectric layer covering the plurality of metal interconnect structures;~~

forming a passivation structure over the plurality of metal interconnect structures, wherein the passivation structure comprises a first dielectric layer and a silicon-oxy-nitride (SiOxNy) layer; and

forming a second dielectric layer over the surface of the silicon-oxy-nitride layer;

wherein the first dielectric is formed by depositing a HDP oxide over the interconnect structure with high density plasma chemical vapor deposition (HDPCVD), and the thickness of the first dielectric layer is substantially between 7000 to 10000Å so as to perform passivation function.

2-3. (Cancelled)

4. (Original) The method as claimed in claim 1, wherein the second dielectric layer is formed by depositing phosphorous silica glass over the silicon-oxy-nitride layer with atmospheric pressure chemical vapor deposition (APCVD).

5. (Original) The method as claimed in claim 4, wherein the thickness of the second dielectric layer is between 8000 to 10000 Å.

6. (Original) The method as claimed in claim 1, wherein the silicon-oxy-nitride (SiOxNy) layer is formed by chemical vapor deposition.

7. (Original) The method as claimed in claim 1, wherein the thickness of the silicon-oxy-nitride (SiOxNy) layer is between 4000 to 7000Å.

8. (Original) The method as claimed in claim 1, wherein the memory device is a flash memory device.

9. (Original) The method as claimed in claim 1, wherein the memory device is a mask ROM.

10. (Original) The method as claimed in claim 1, wherein the first dielectric layer is thicker than or equal to the silicon-oxy-nitride (SiO_XN_Y) layer.

11. (Original) The method as claimed in claim 1, wherein at least one of the first dielectric layer, the silicon-oxy-nitride (SiO_XN_Y) layer, or the second dielectric layer comprises a substantially planarized surface.

12. (Previously Presented) A method for forming a passivation layer on a memory device with an interconnect structure thereon, comprising:

forming a first dielectric layer over the surface of the interconnect structure;

forming a silicon-oxy-nitride (SiOxNy) layer over the surface of the first dielectric layer; and

forming a second dielectric layer over the surface of the silicon-oxy-nitride layer;

wherein the interconnect structure comprises a metal interconnect layer and a substantially planarized inter-layered dielectric layer covering the metal interconnect layer; and

wherein the memory device comprises a charge loss in a range of approximately 0.060 to 0.096 and a standard deviation in a range of approximately 0.108 to 0.047.

13. (Previously Presented) The method as claimed in claim 12, wherein the first dielectric layer is formed by depositing a HDP oxide over the interconnect structure with high density plasma chemical vapor deposition (HDPCVD).

14. (Previously Presented) The method as claimed in claim 13, wherein the thickness of the first dielectric layer is between 7000 to 10000Å.

15. (Previously Presented) The method as claimed in claim 12, wherein the second dielectric layer is formed by depositing phosphorous silica glass over the silicon-oxy-nitride layer with atmospheric pressure chemical vapor deposition (APCVD).

16. (Previously Presented) The method as claimed in claim 15, wherein the thickness of the second dielectric layer is between 8000 to 10000 Å.

17. (Previously Presented) The method as claimed in claim 12, wherein the silicon-oxy-nitride (SiOxNy) layer is formed by chemical vapor deposition.

18. (Previously Presented) The method as claimed in claim 12, wherein the thickness of the silicon-oxy-nitride (SiOxNy) layer is between 4000 to 7000Å.

19. (Previously Presented) The method as claimed in claim 12, wherein the memory device is a flash memory device.

20. (Previously Presented) The method as claimed in claim 12, wherein the memory device is a mask ROM.

21. (Previously Presented) The method as claimed in claim 12, wherein the first dielectric layer is thicker than or equal to the silicon-oxy-nitride (SiO_XN_Y) layer.

22. The method as claimed in claim 12, wherein at least one of the first dielectric layer, the silicon-oxy-nitride (SiO_XN_Y) layer, or the second dielectric layer comprises a substantially planarized surface.

23. (Cancelled)

24. (Previously Presented) The method as claimed in claim 1, wherein the substantially planarized inter-layered is made of a hydrogen blocking material.

25. (New) The method as claimed in claim 1, further comprising forming a substantially planarized inter-layered dielectric layer covering the plurality of metal interconnect structures.